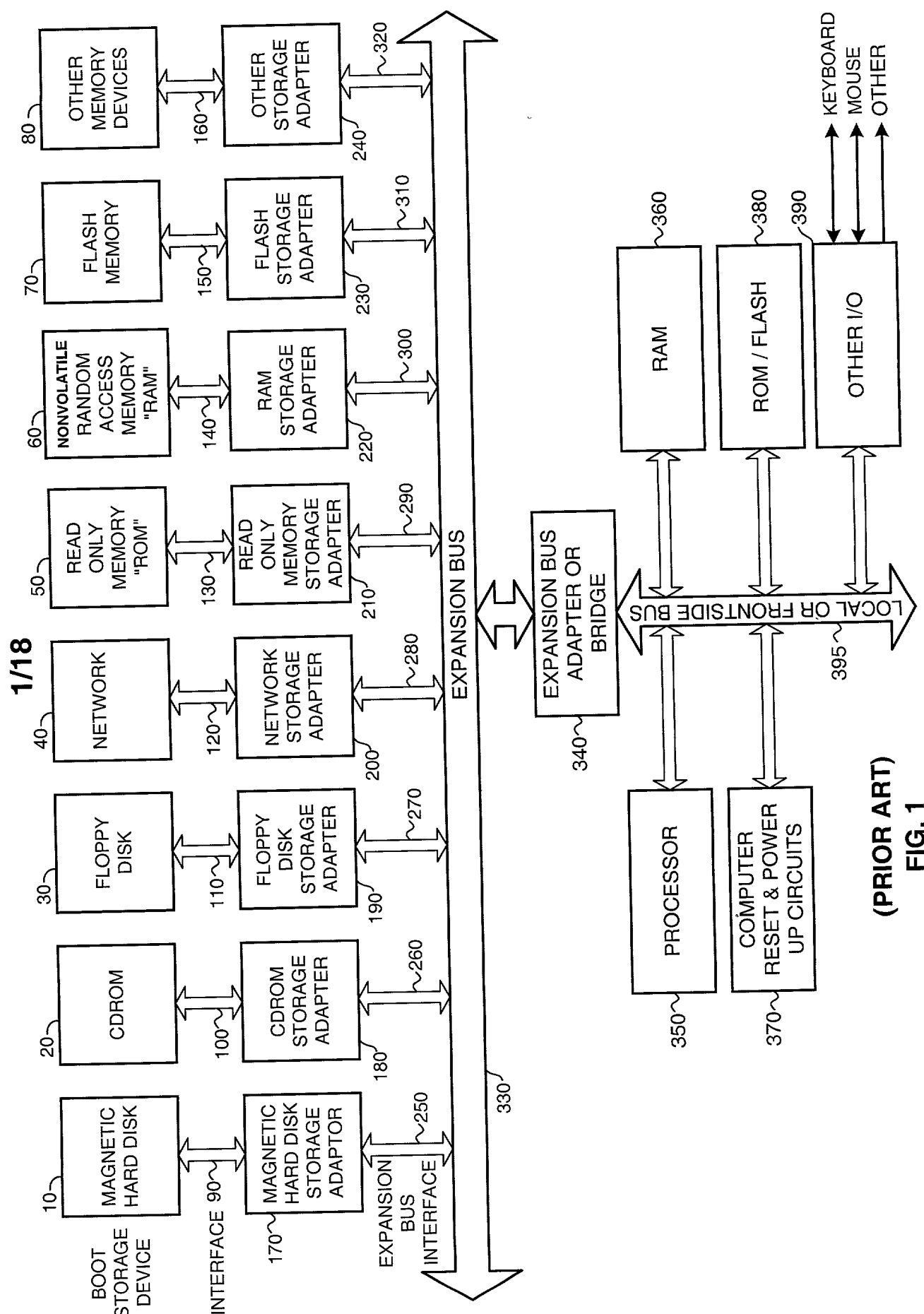
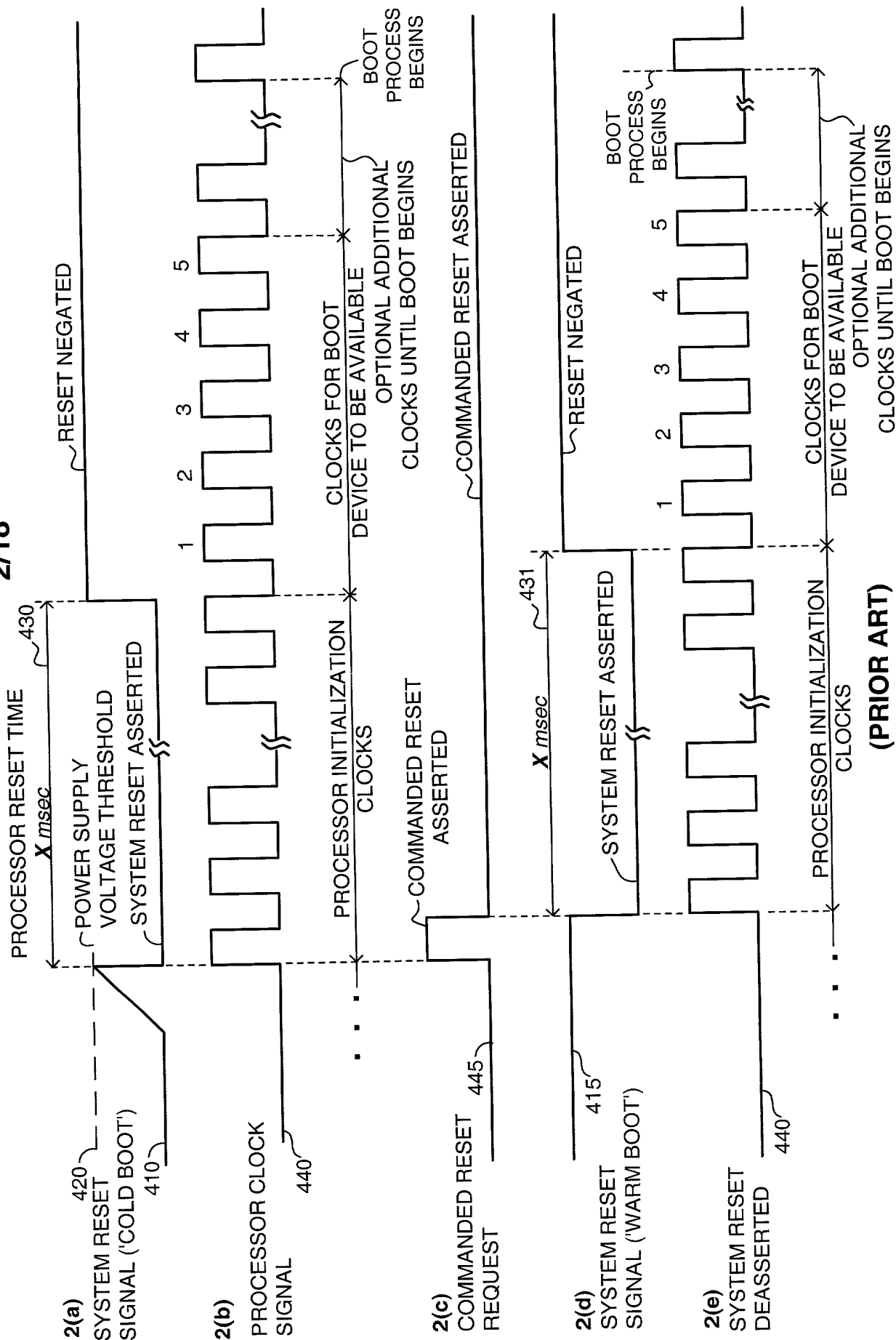


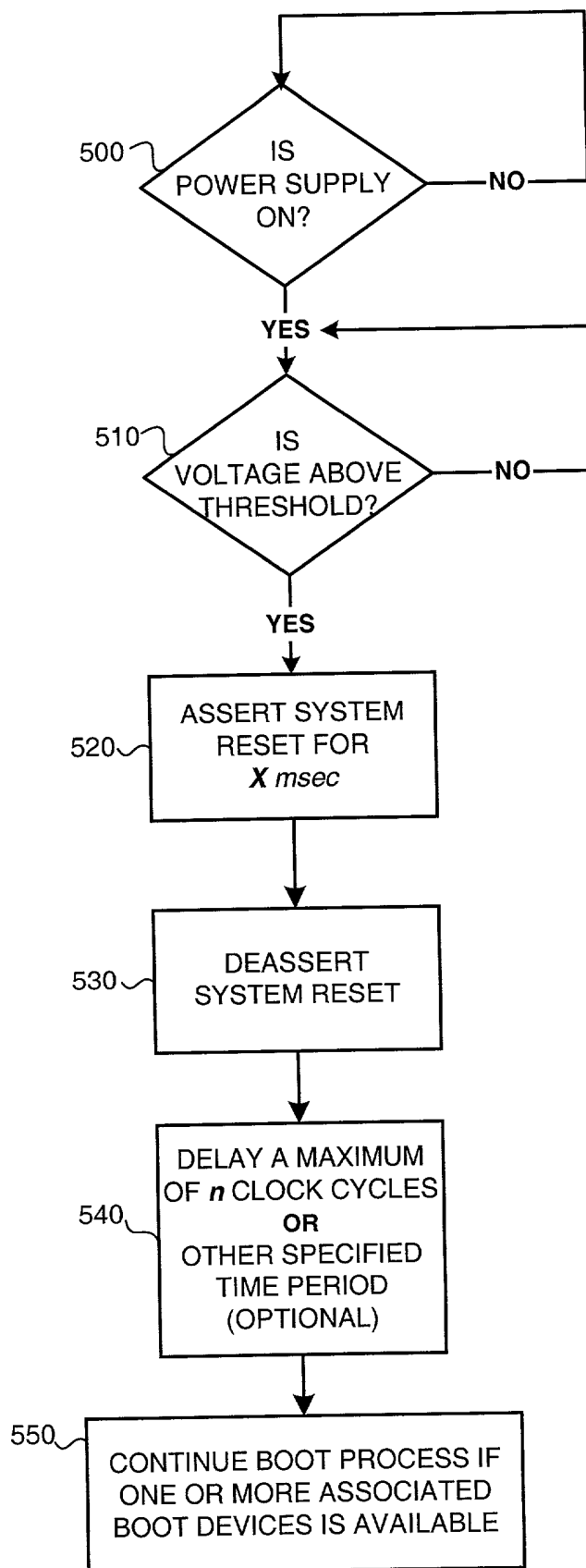
1/18



(PRIOR ART)  
FIG. 1

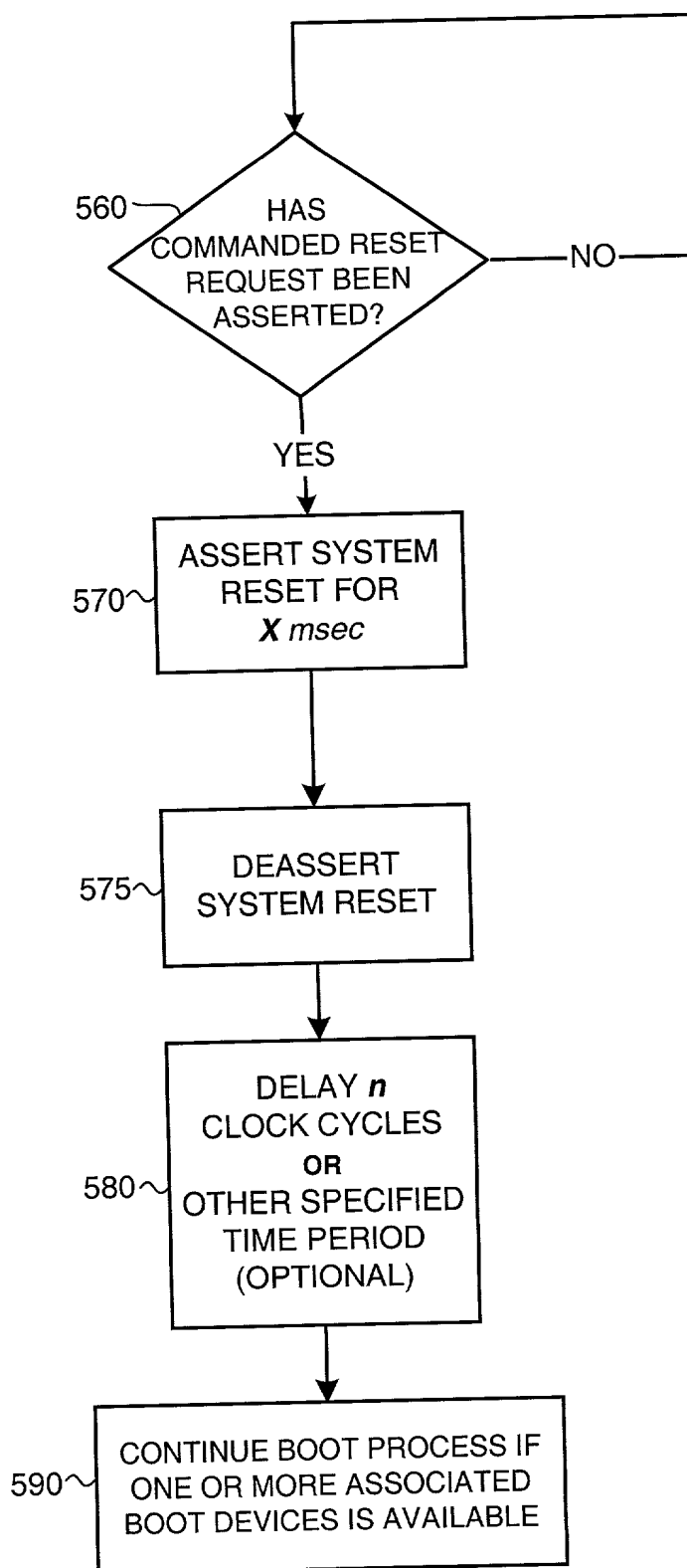


(PRIOR ART)  
FIG. 2



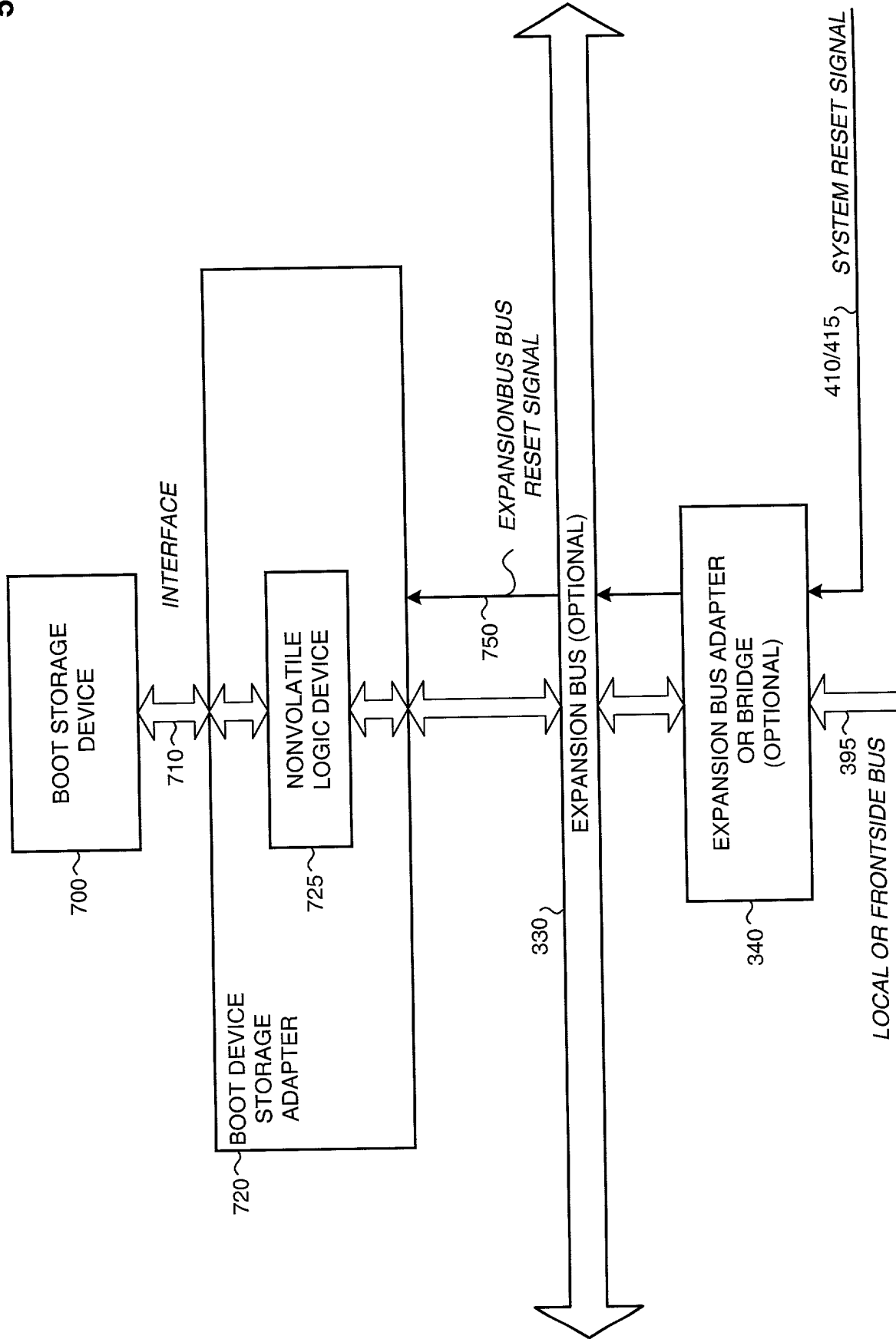
(PRIOR ART)

FIG. 3a



(PRIOR ART)

FIG. 3b



(PRIOR ART)  
FIG. 4

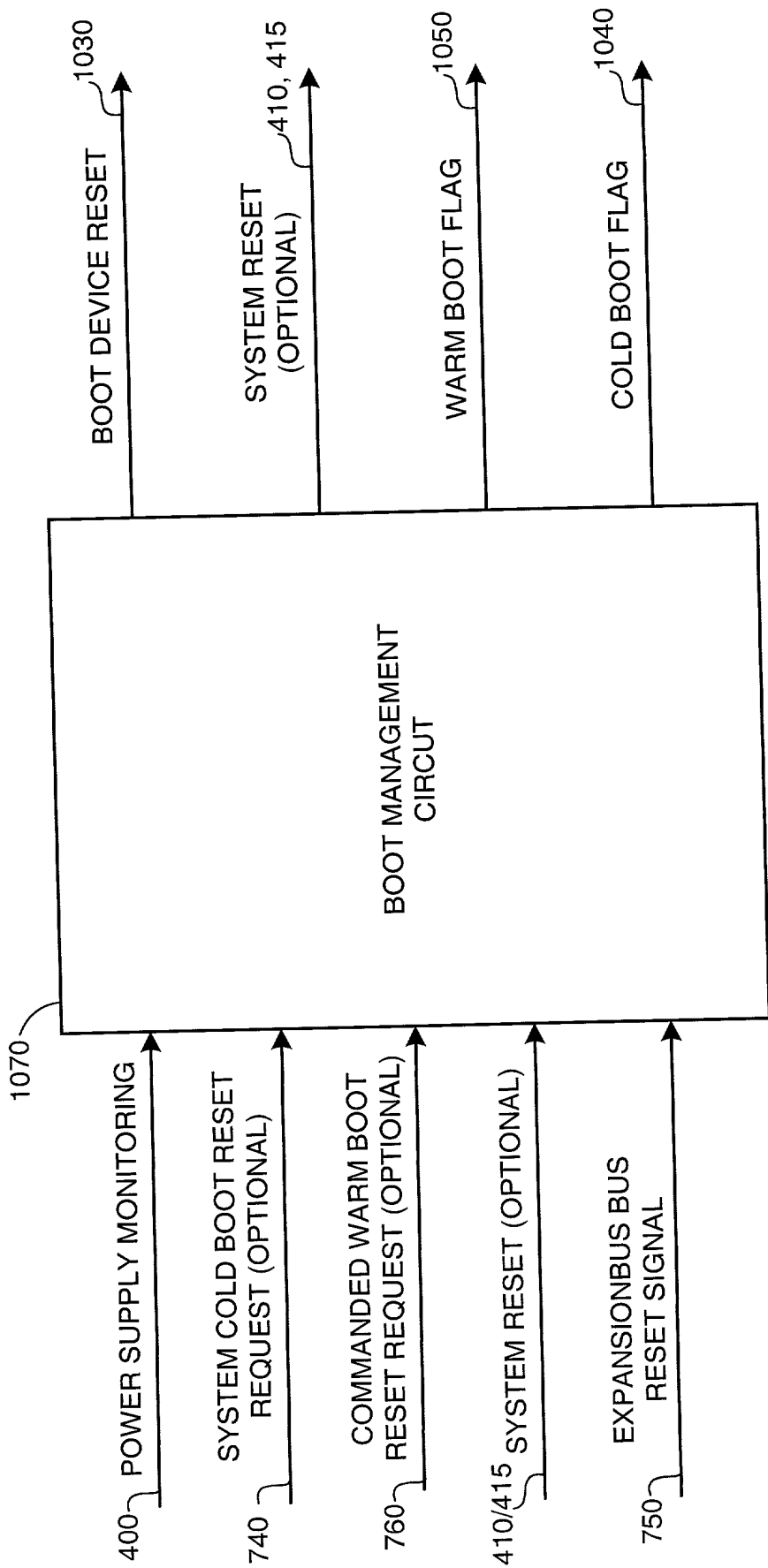


FIG. 5

FIG. 6 is a timing diagram showing the sequence of events during a system reset. The diagram includes signals for operating voltage, power supply monitoring, system reset signal, processor clock, boot device reset, cold boot flag, and warm boot flag. Key time intervals are labeled: X msec for processor reset time, Y msec for system reset signal duration, and Z msec for boot device reset duration. The diagram also shows the number of clocks for boot device to be available (n) and the boot process begins.

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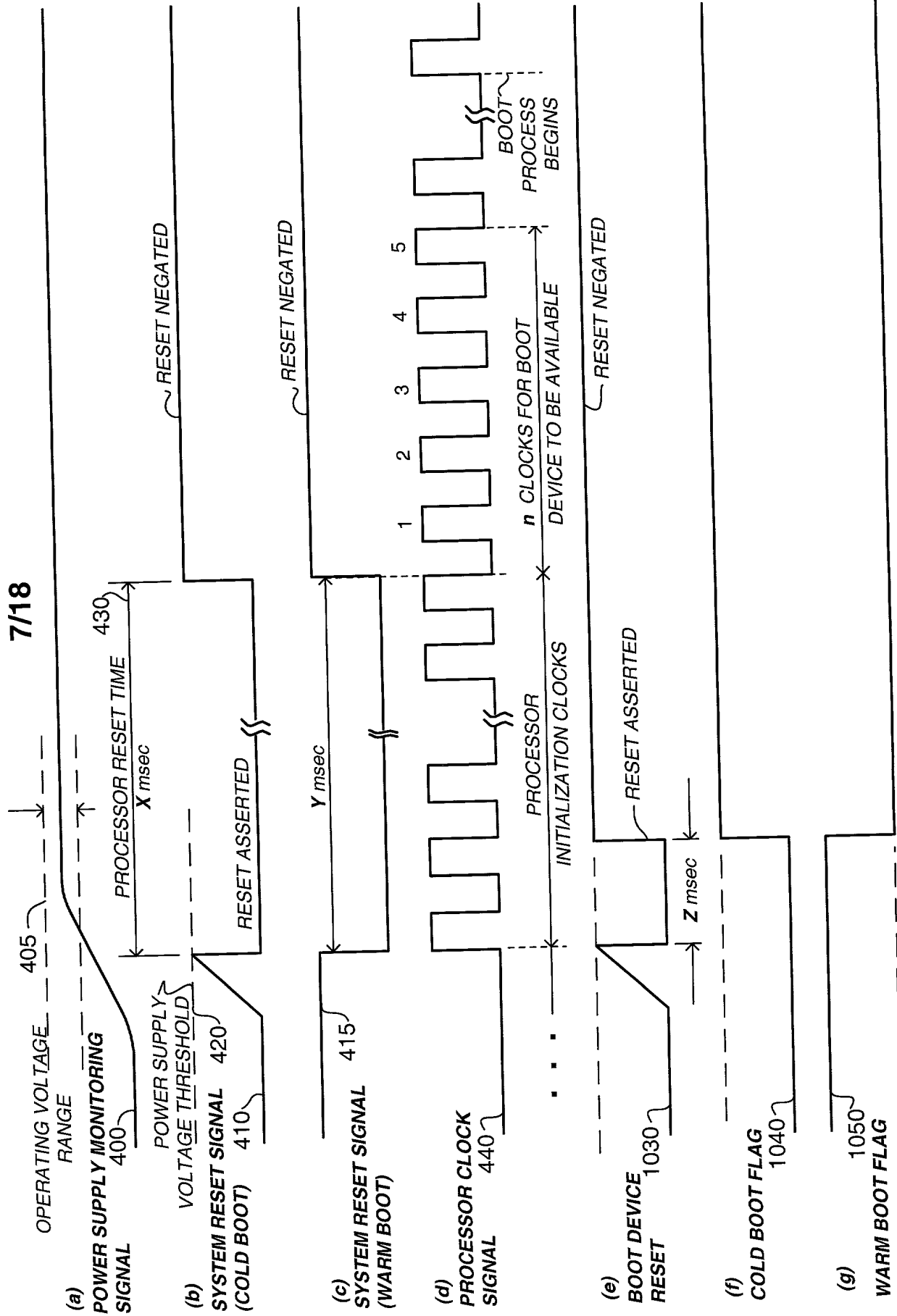
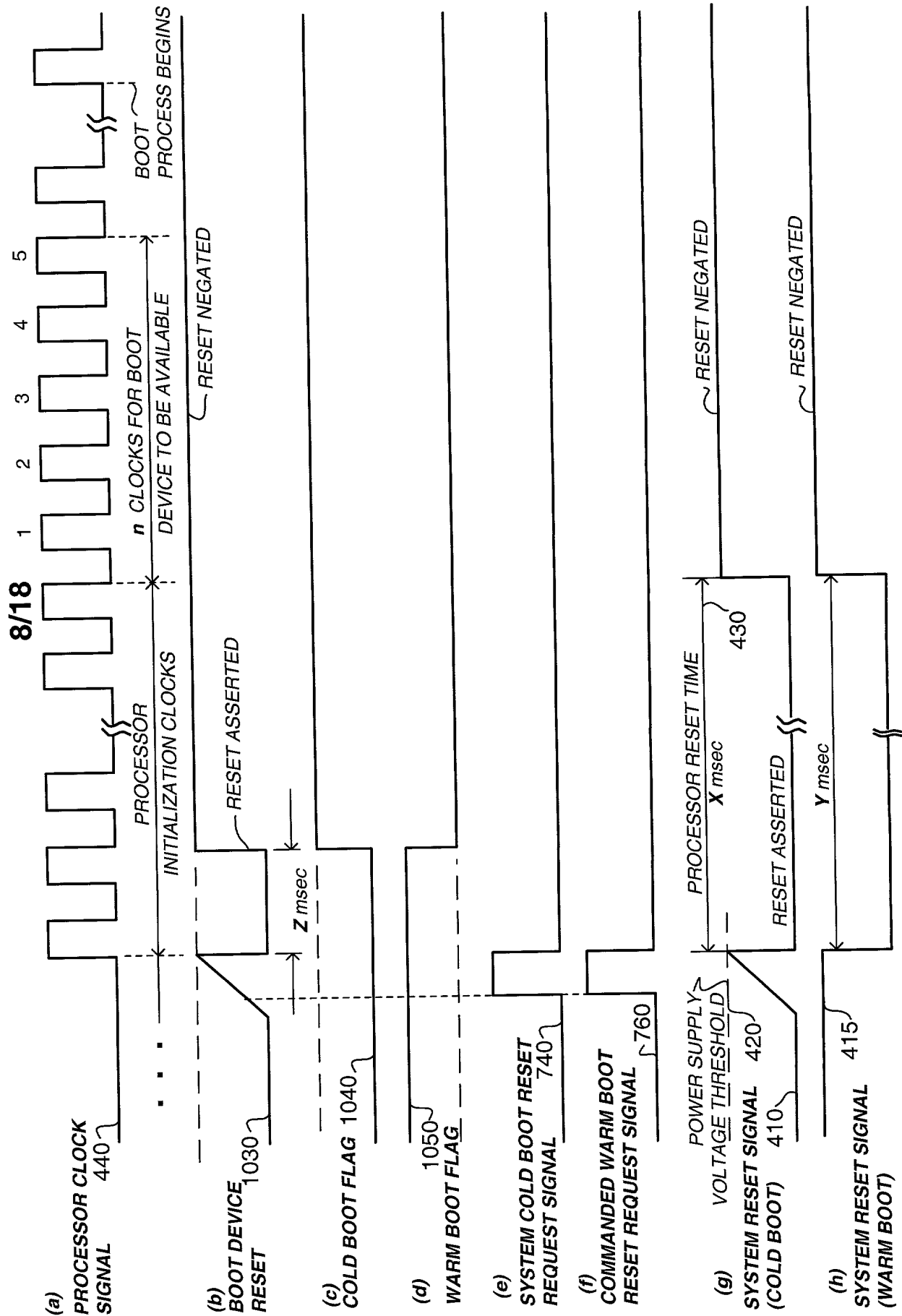


FIG. 6

When the reset signal is asserted, the processor clock is stopped. The reset signal is asserted for a period of time that is long enough to ensure that the processor is reset.



**FIG. 7**



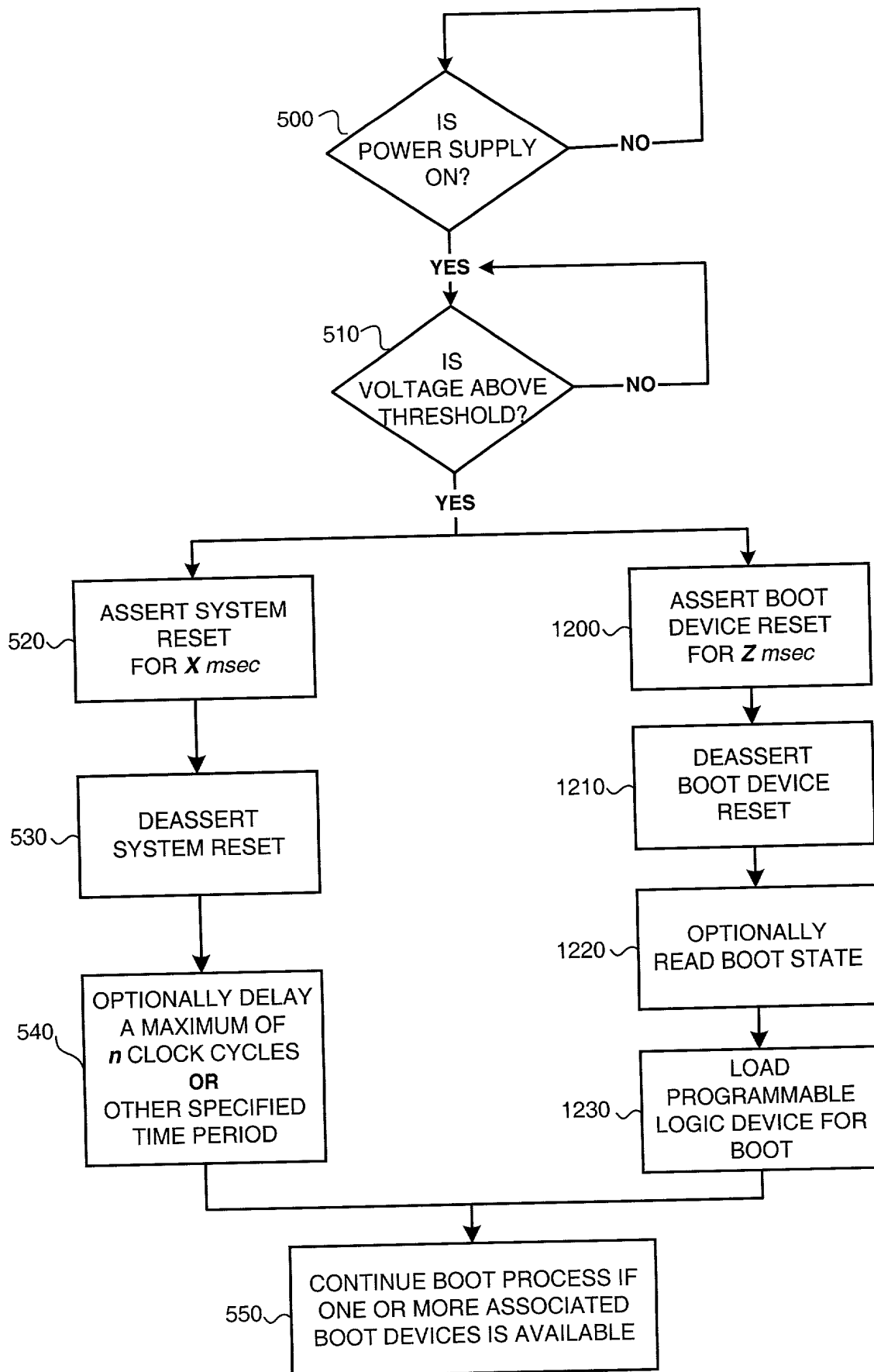


FIG. 8a

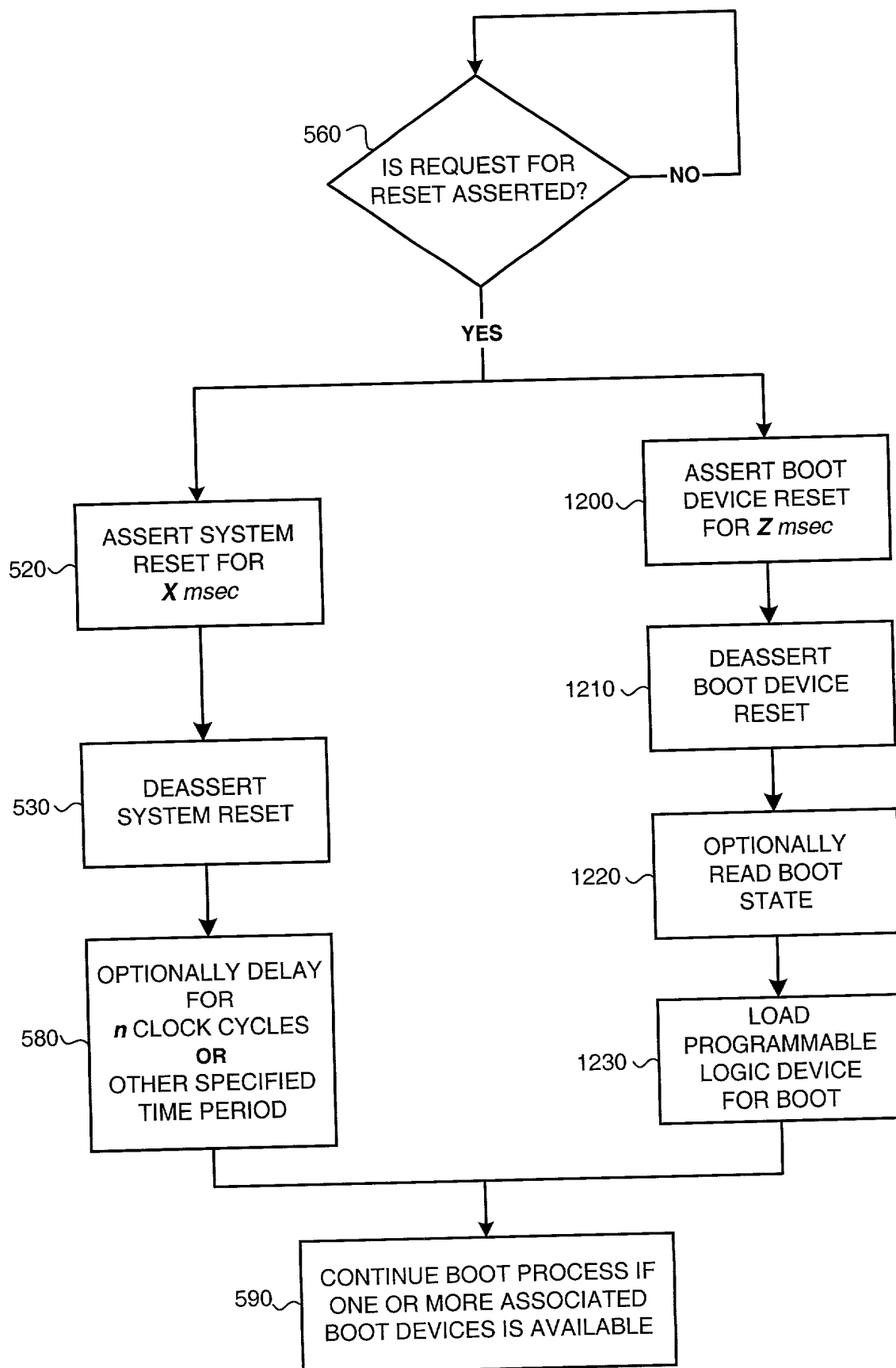


FIG. 8b

POWER SUPPLY MONITORING

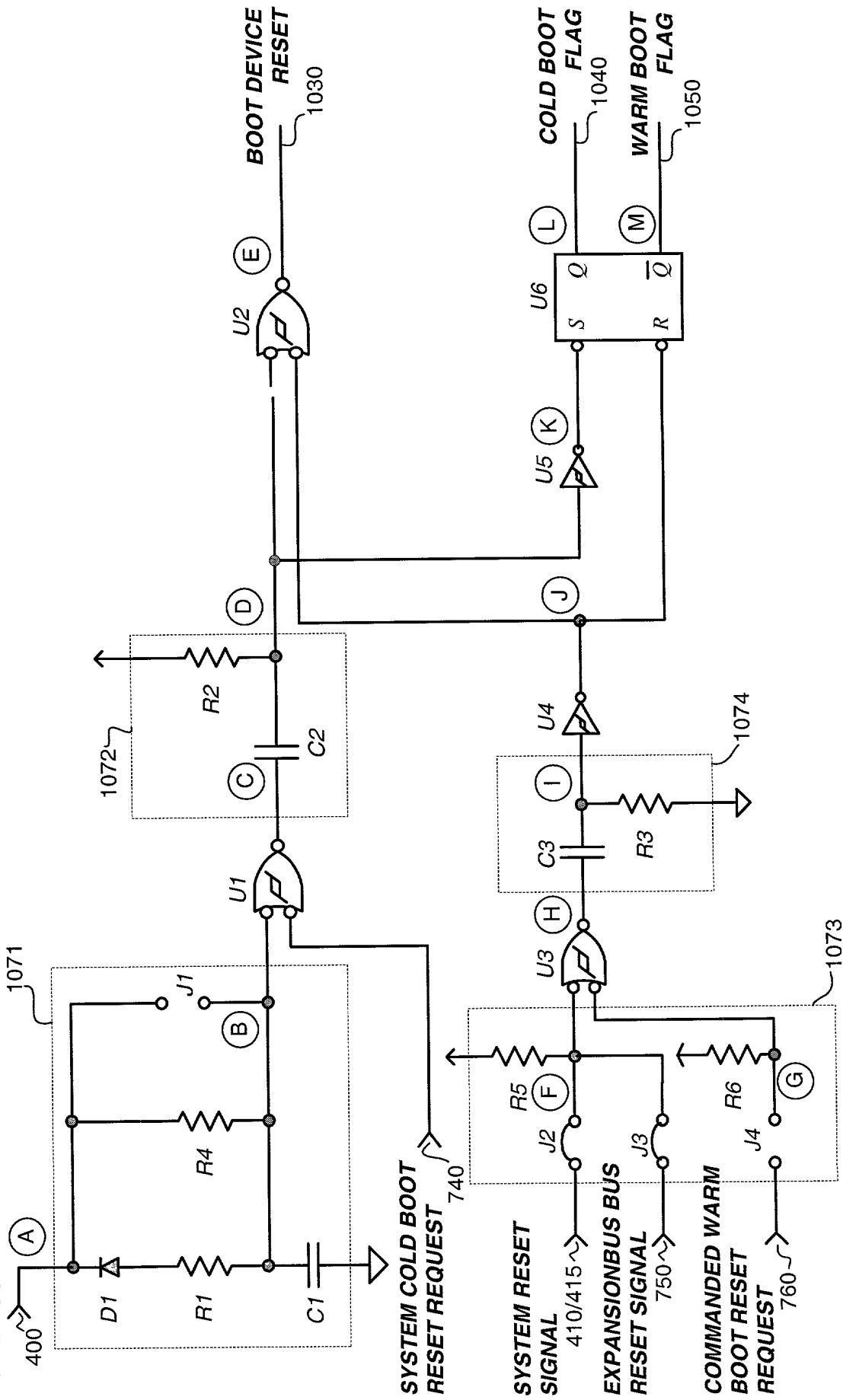
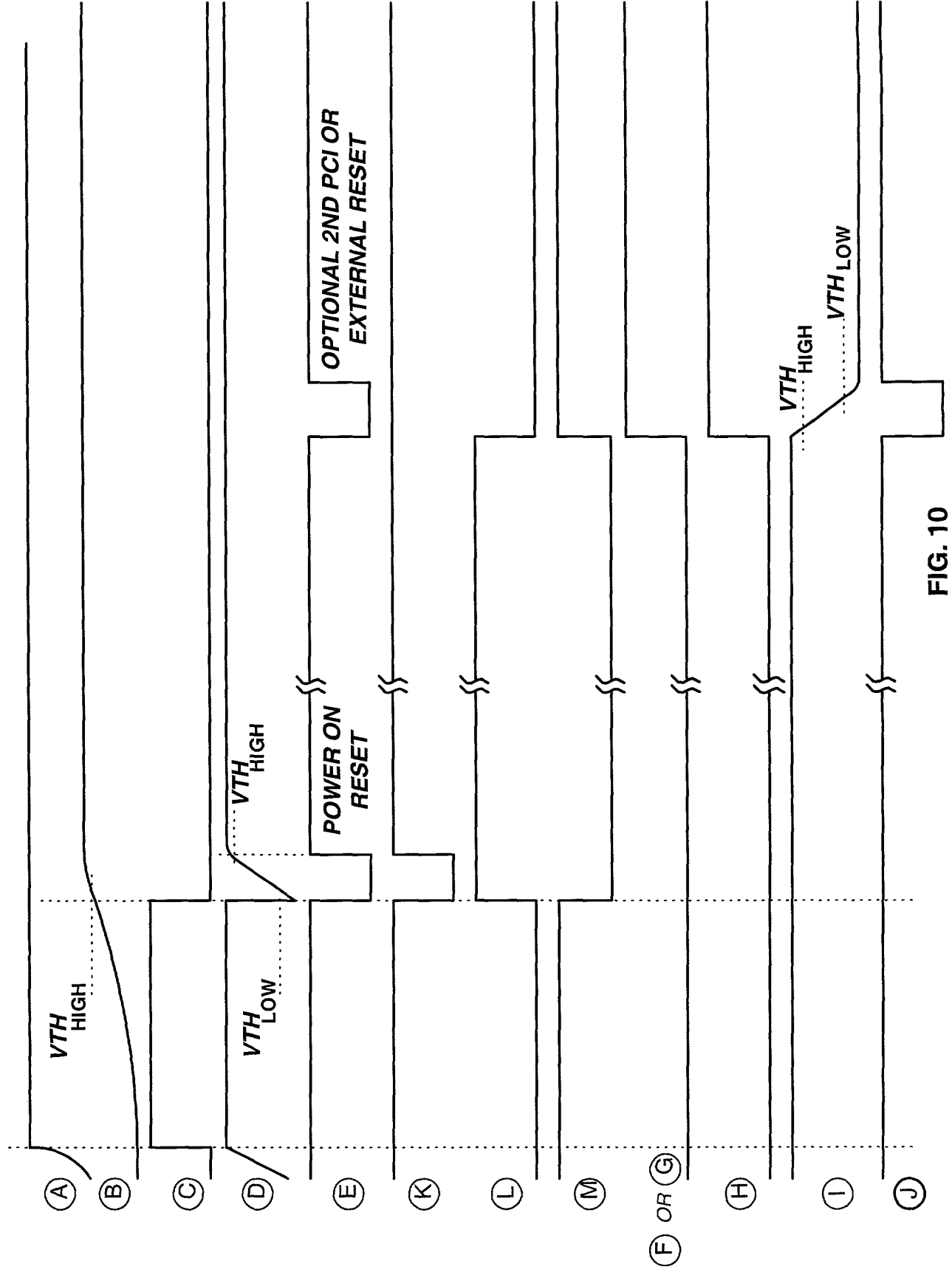


FIG. 9



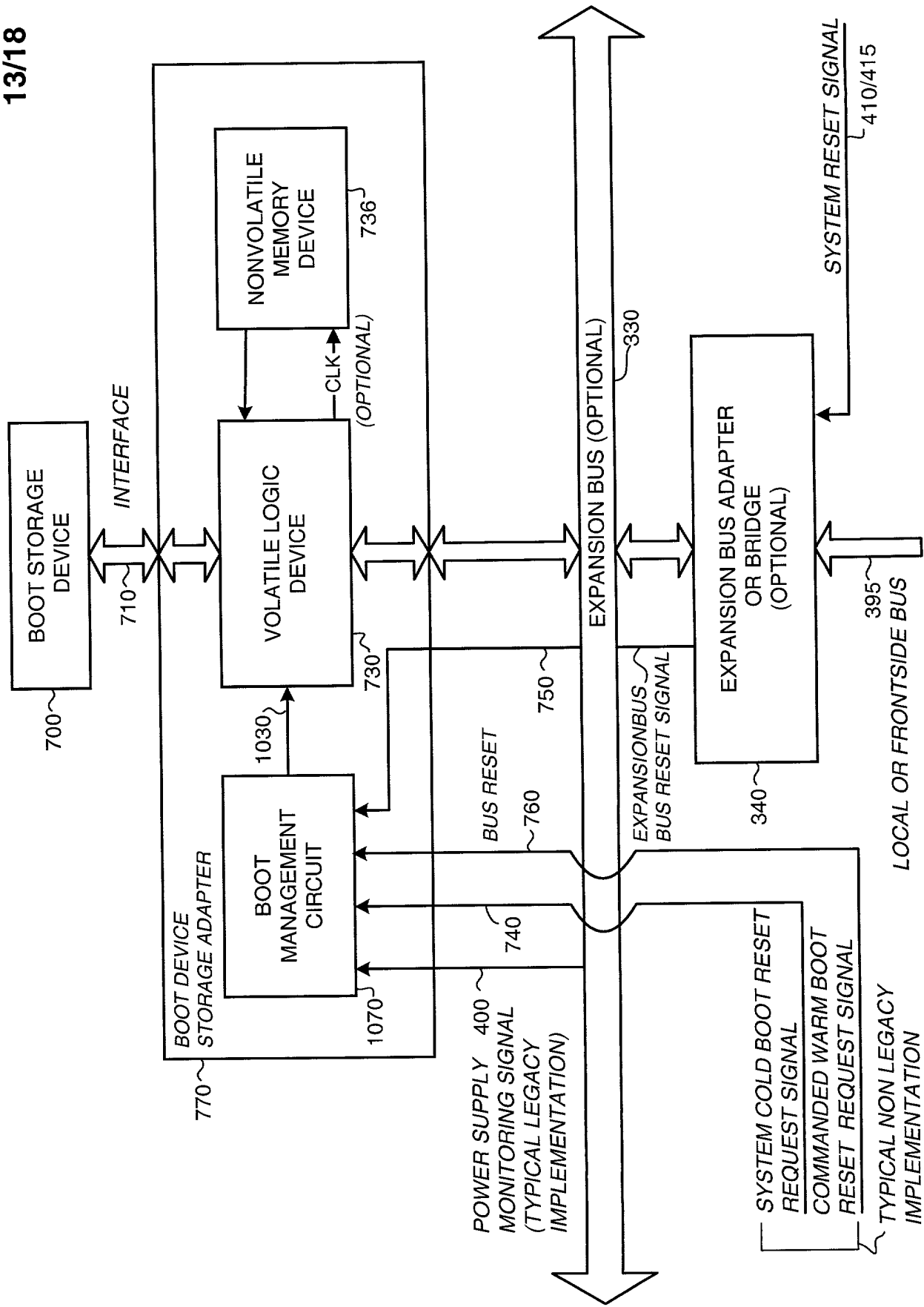


FIG. 11

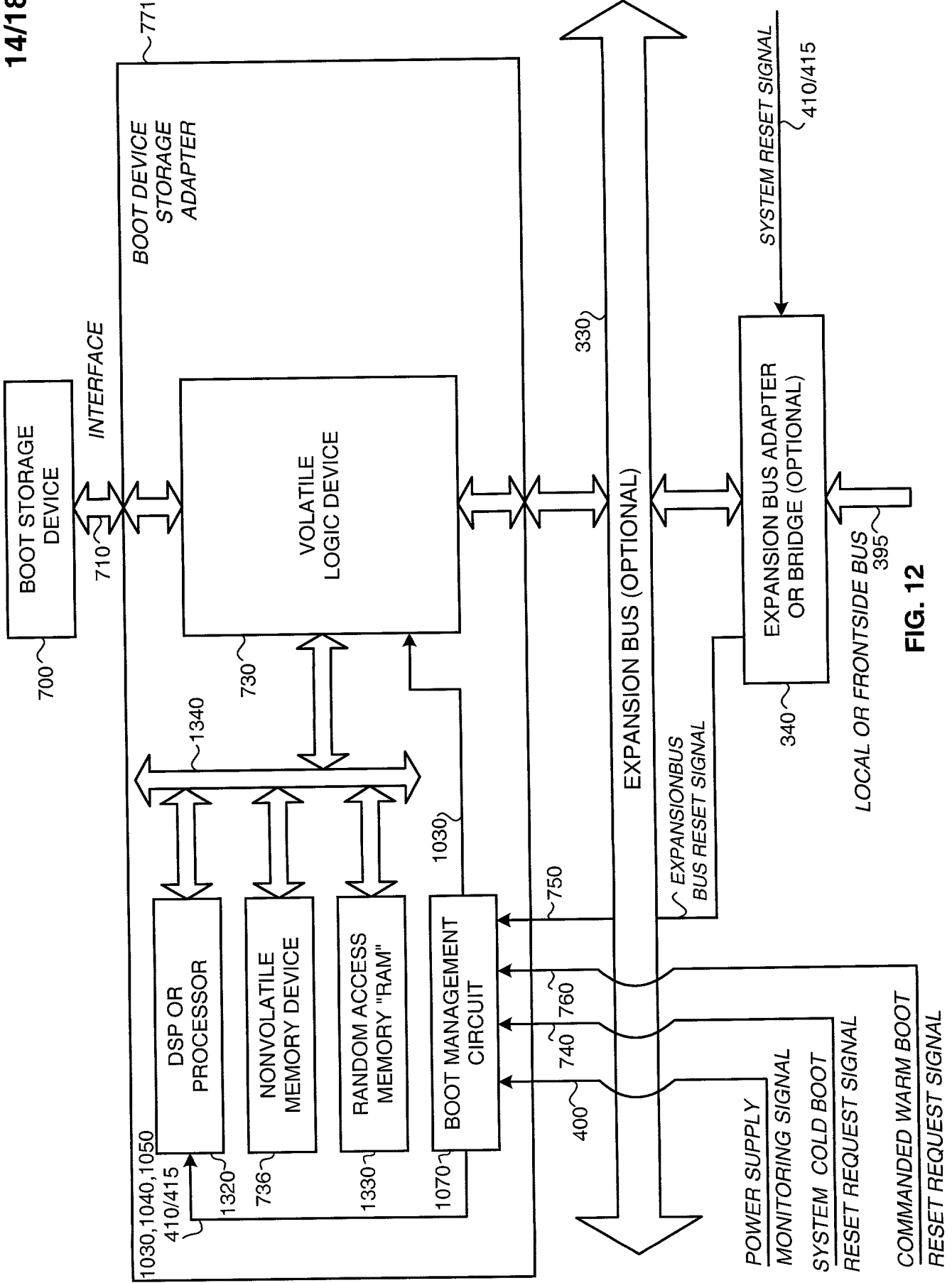


FIG. 12

FIG. 13 is a block diagram of a system architecture for a boot device. The system includes a boot management circuit 1070, a boot storage device 700, a volatile logic device 730, a nonvolatile memory device 795, and an expansion bus 330. The boot management circuit 1070 is connected to the boot storage device 700 via an interface 710. The boot storage device 700 is connected to the volatile logic device 730 via a boot device storage adapter 772. The volatile logic device 730 is connected to the nonvolatile memory device 795 via a system reset signal 410/415. The expansion bus 330 is connected to the boot management circuit 1070, the volatile logic device 730, and the nonvolatile memory device 795. The expansion bus 330 also includes an optional expansion bus adapter or bridge 340, which is connected to a local or frontside bus 395. The local or frontside bus 395 is connected to a nonvolatile memory device 785. The expansion bus 330 also includes a power supply monitoring signal 400, a system cold boot reset request signal 1030, 1040, 1050, 410/415, and a commanded warm boot reset request signal 1030, 1040, 1050, 410/415.

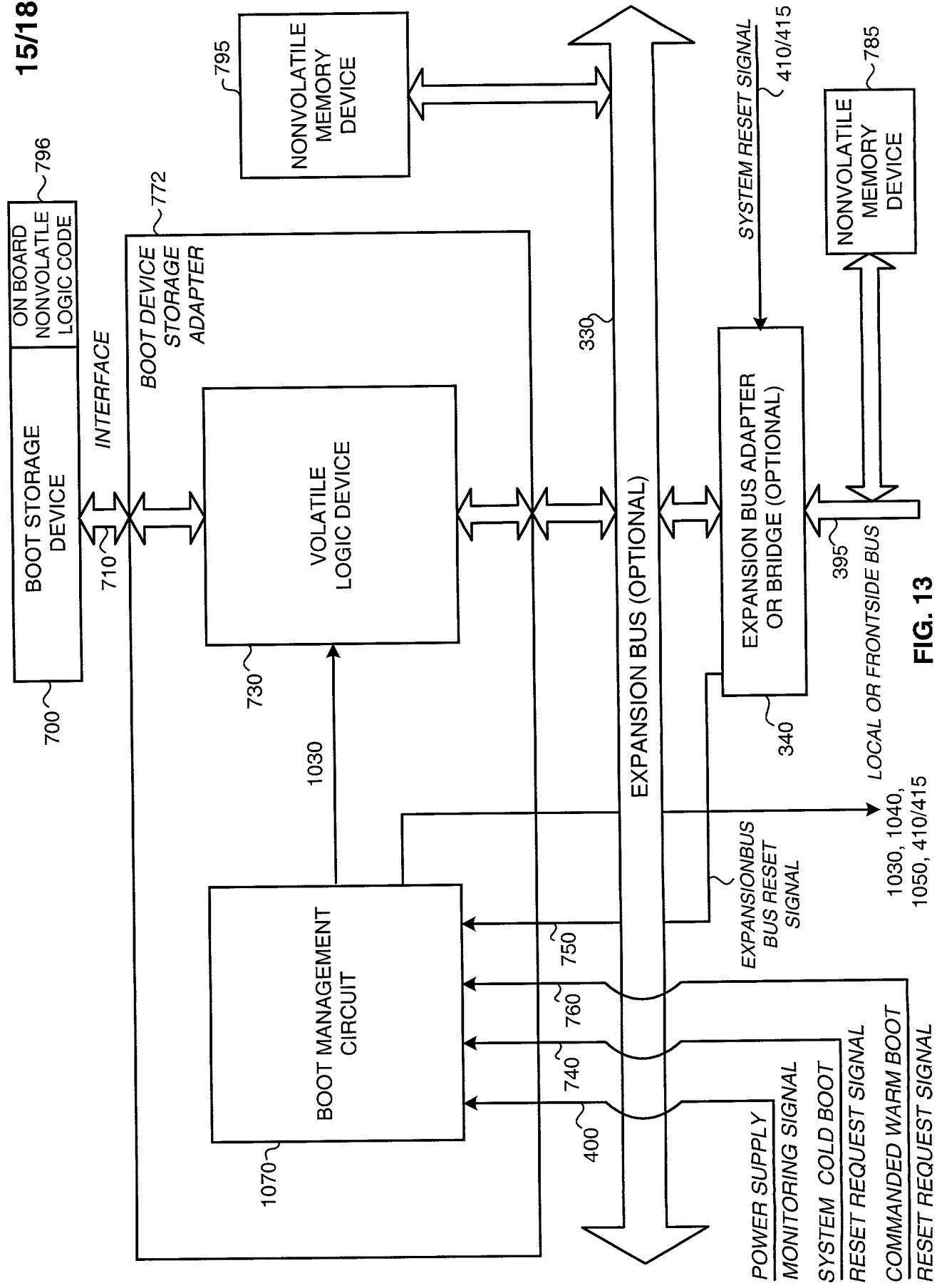


FIG. 13

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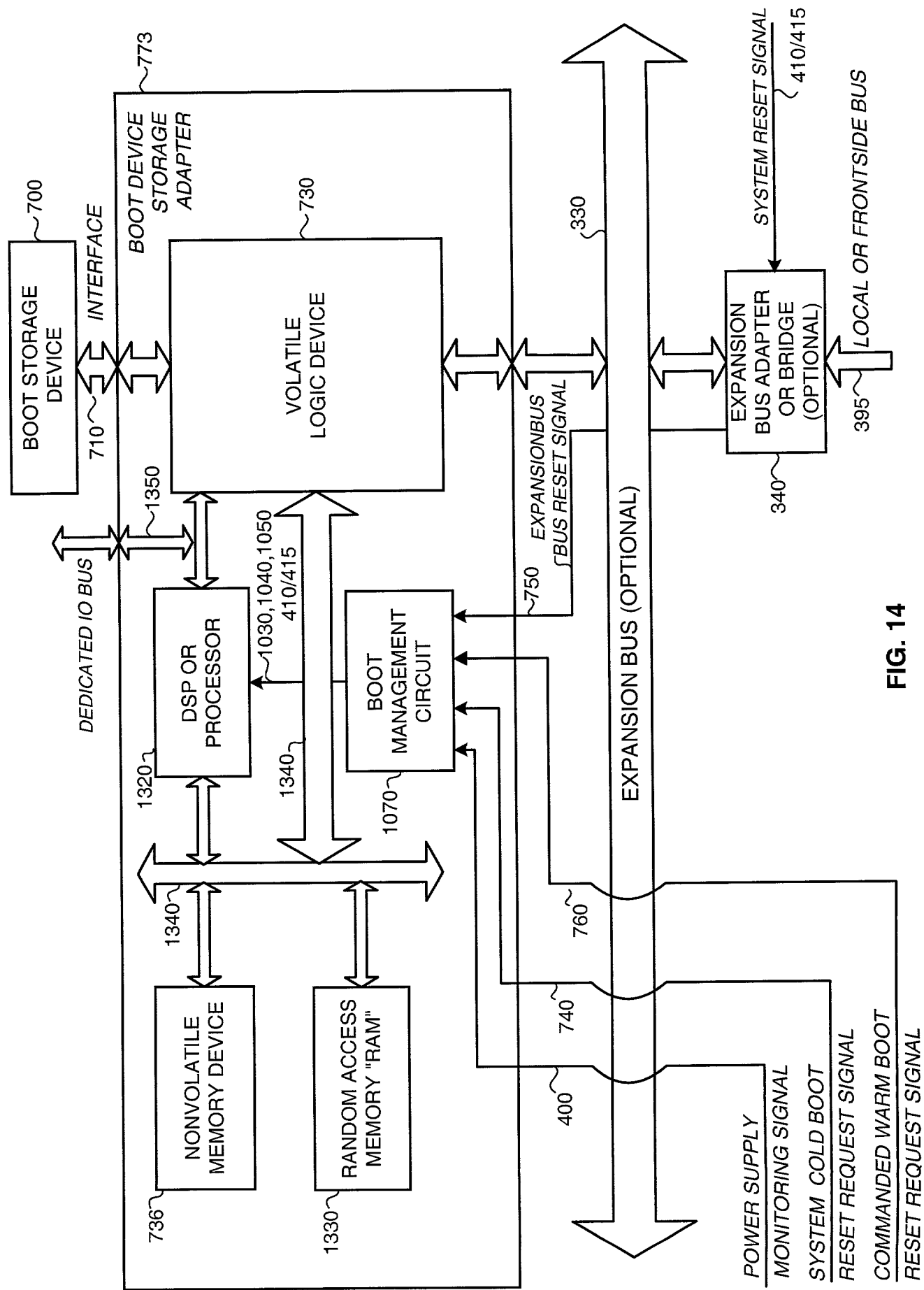


FIG. 14



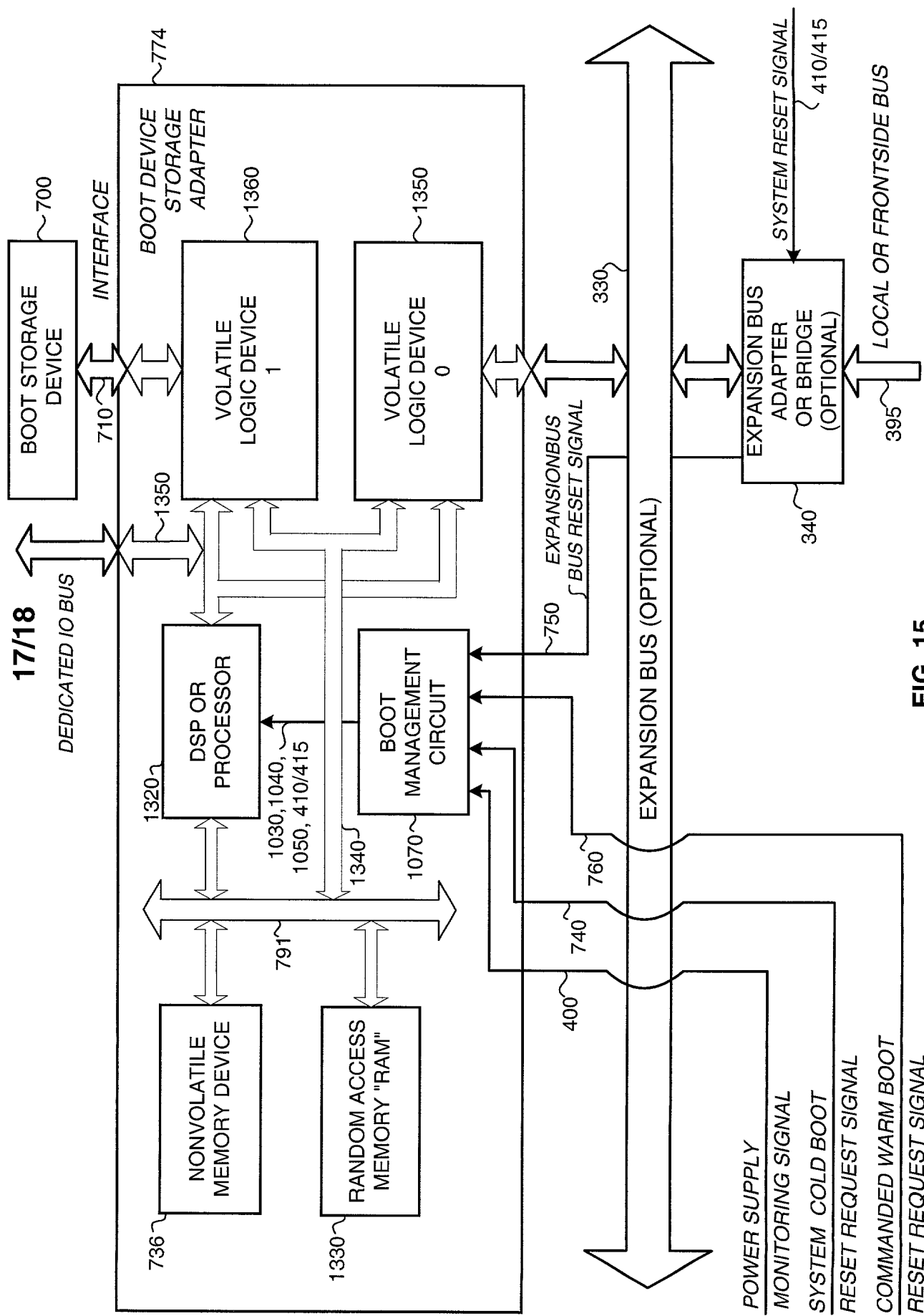


FIG. 15

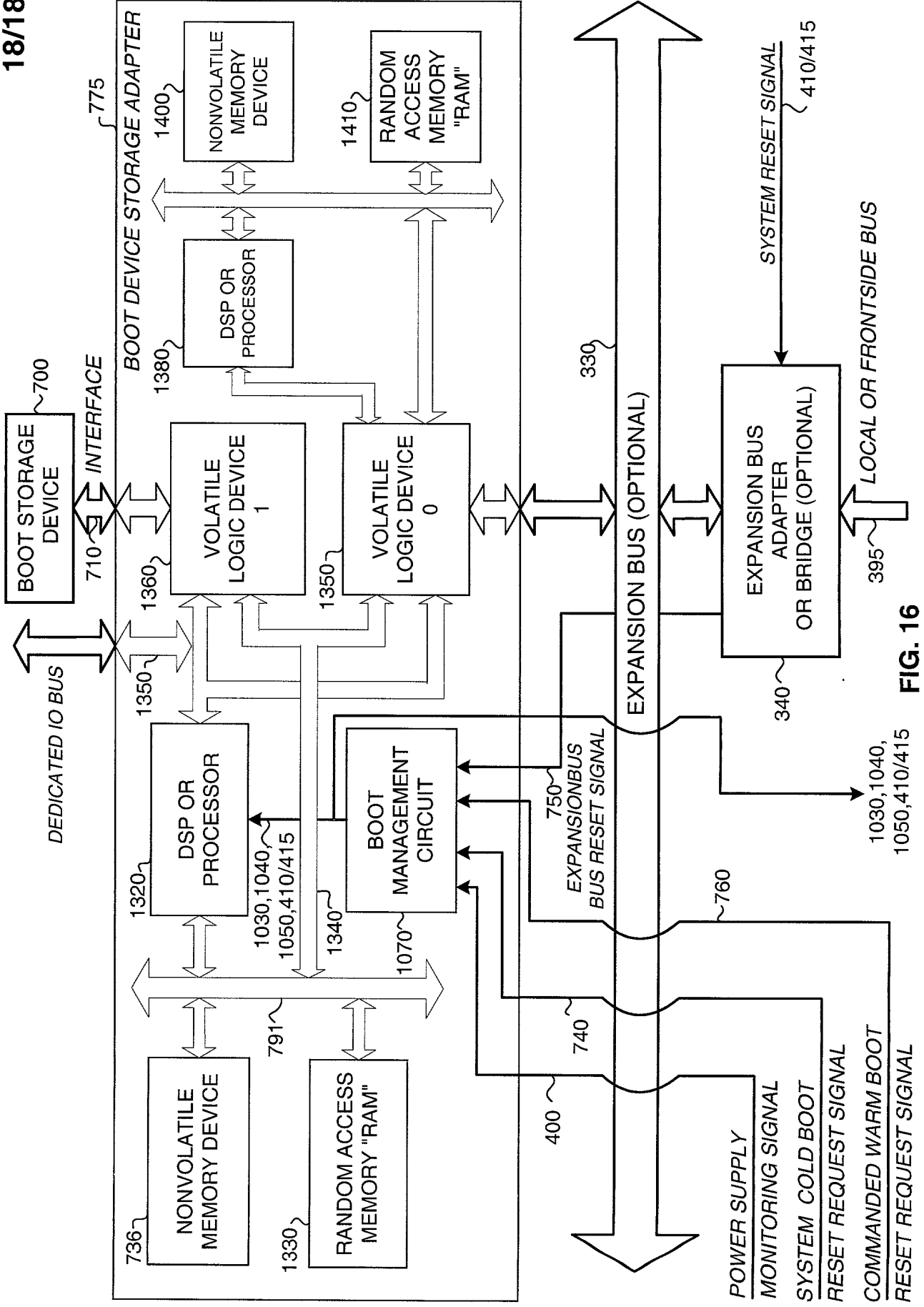


FIG. 16